REMARKS

Claims 1-3 and 5-14 are pending in this application. By this Amendment, the specification and claims 1-2, 7, 9-10 and 12 are amended. Various amendments are made for clarity and are unrelated to issues of patentability.

Entry of the amendments is proper under 37 C.F.R. §1.116 because the amendments: (1) place the application in condition for allowance for the reasons set forth below; (2) do not raise any new issues requiring further search and/or consideration; and/or (3) place the application in better form for appeal (if necessary). More specifically, the above amendments are merely for clarity and do not raise any new issues. Entry is therefore proper under 37 C.F.R. §1.116.

The Office Action objects to claims 1 and 9 because of informalities. It is respectfully submitted that the above amendments obviate the grounds for objection. Withdrawal of the objection is respectfully requested.

The Office Action rejects claims 1-3 and 5-14 under 35 U.S.C. §103(a) over U.S. Patent 6,480,529 to Sih et al. (hereafter Sih), U.S. Patent 6,724,807 to Krasner et al. (hereafter Krasner) and in further view of U.S. Patent 6,333,926 to Van Heeswyk et al. (hereafter Van Heeswyk). The rejection is respectfully traversed with respect to the pending claims.

Independent claim 1 recites a first shift register bank and a second shift register bank, wherein the input signals of an even path are sampled in a first half PN chip and the input signals of an odd path are sampled in a following half PN chip. Independent claim 1 also recites first despreading means for despreading the input signals of the even path using the PN codes inputted from the first shift register bank, wherein the first despreading means despreads the

input signals of the even path in parallel to output first despreading signals, and second despreading means for despreading the input signals of the odd path using the PN codes inputted from the first shift register bank, wherein the second despreading means despreads the input signals of the odd path in parallel to output second despreading signals. Still further, independent claim 1 recites a coherent accumulator, energy calculation means, and a non-coherent accumulator.

The present specification describes a non-limiting example of a despreading circuit 50 that includes a first despreading circuit 52 and a second despreading circuit 53. See paragraph [31]. As expressly stated in the one example, the first despreading unit 52 and the second despreading unit 53 output 32 despreaded results in the I component type and 32 despreaded results in the Q component type, which are received by the coherent accumulator 34, respectively. See also paragraph [32] describing the coherent accumulator 34 receiving 64 pairs of the despread signals.

The applied references do not teach or suggest at least these features of independent claim 1. More specifically, the Office Action (on page 5) states that Sih and Krasner do not disclose the claimed first despreading means and second despreading means, wherein the first despreading means despreads the input signal of the even path in parallel to output first despreading signals and wherein the second despreading means despreads the input signals of the odd path in parallel to output second despreading signals.

The Office Action relies on Van Heeswyk as teaching the missing features of independent claim 1 relating to input signals of the even and odd paths and the first and second

dispreading means. More specifically, the Office Action cites Van Heeswyk's PNi and PNq spreading elements 270, 272 as corresponding to the claimed first despreading means and cites Van Heeswyk's PNi and PNq spreading elements 274, 276 as corresponding to the claimed second despreading means. See Van Heeswyk's col. 11, lines 15-20. The Office Action also asserts that Van Heeswyk's col. 11, lines 15-18 and lines 20-29 teach that the first despreading means despreads the input signals of the even path in parallel to output first despreading signals and the second despreading means despreads the input signals of the odd path in parallel to output second despreading signals.

Van Heeswyk's FIG. 5C shows that adder 278 outputs an I signal based on outputs of the spreading elements 270, 276 and adder 280 outputs a Q signal based on outputs of the spreading elements 272, 274. Thus, Van Heeswyk does not teach or suggest that the claimed first despreading means despreads the input signals of the even path in parallel to output first despreading signals and the claimed second despreading means despreads the input signals of the odd path in parallel to output second despreading signals. Van Heeswyk does not despread input signals in parallel to output despread signals. Accordingly, the applied references do not teach or suggest all the features of independent claim 1. Additionally, Van Heeswyk does not suggest the missing features of the input signals of an even path are sampled in a first half PN chip, the input signals of an odd path are sampled in a following half in combination with the claimed first despreading means and second despreading means.

When discussing dependent claim 5, the Office Action also cites Sih's FIG. 6C and QPSK despread 804a and 804b as corresponding to the first despreading means and the second

despreading means. However, these features do not correspond to elements within Van Heeswyk's PN spreading block 262. Additionally, Sih's FIG. 6C does not suggest the claimed input signals of an even path are sampled in a first half PN chip and input signals of an odd path are sampled in a following half chip. There is no suggestion to modify Sih's FIG. 6C to include these missing features with Sih's QPSK despread 804a and 804b. Further, there is no suggestion to modify Sih's FIG. 6C so as to include the features of Van Heeswyk's FIG. 5C. For example, there is no suggestion to modify Sih's FIG. 5C to include a PN spreading block 262 that includes an I signal output from adder 278 and a Q signal output from adder 280.

The Office Action also states that Sih does not teach the claimed first shift register bank that sequentially stores PN codes and the claimed second shift register bank that sequentially stores input signals. When discussing the claimed second shift register, the Office Action (on page 4) references Krasner's FIG. 2, elements 400, 402. However, Krasner does not include any elements 400 or 402.

Applicant further submits that the alleged combination of Sih, Krasner and Van Heeswyk is clearly based on impermissible hindsight as there is no suggestion to combine the references. The only suggestion to combine features is based on applicant's disclosure. Additionally, applicant respectfully submits that the Office Action fails to make a *prima facie* case of obviousness since: (a) the references as a whole do not teach or suggest all the features of independent claim 1, and (b) the references may not be properly combined as alleged. Accordingly, independent claim 1 defines patentable subject matter.

Independent claim 9 recites that the input signals of an even path are sampled in a first half PN chip and the input signals of an odd path are sampled in a following half PN chip. Independent claim 9 also recites despreading the set of input signals of the even path in parallel by using the PN codes, despreading the set of input signals of the odd path in parallel by using the PN codes, and outputting an accumulation signal by accumulating despreaded signals of the even path and despreaded signals of the odd path.

For at least similar reasons as set forth above, the applied references do not teach or suggest at least these features of independent claim 9. More specifically, the Office Action (on pages 9-10) states that Sih and Krasner do not teach that input signals of an even path are sampled in a first half PN chip and input signals of the odd path are sampled in a following half chip in combination with despreading the input signals of the even/odd paths in parallel by using the PN codes. The Office Action then relies on VanHeeswyk's FIG. 5C and col. 11, lines 7-29 for these missing features. However, for at least similar reasons as set forth above, Van Heeswyk does not suggest despreading the set of input signals of the even path in parallel by using the PN codes, and despreading the set of input signals of the odd path in parallel by using the PN codes. Thus, independent claim 9 defines patentable subject matter.

For at least the reasons set forth above, each of independent claims 1 and 9 defines patentable subject matter. Each of the dependent claims depends from one of the independent claims and therefore defines patentable subject matter at least for this reason. In addition, the dependent claims recite features that further and independently distinguish over the applied references.

For example, dependent claim 5 recites that the first despreading means and the second despreading means each comprise a plurality of despreading device means that are equal in number to each of the PN codes and the input signals. As discussed above, Sih's Fig. 6C does not correspond to the claimed first despreading means and second despreading means. The Office Action (on page 5) also clearly states that Sih does not disclose the claimed first despreading means and second despreading means. The applied references do not teach or suggest all the features of dependent claim 5. Accordingly, dependent claim 5 defines patentable subject matter at least for this additional reason.

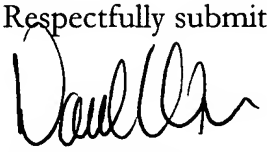
CONCLUSION

In view of the foregoing, it is respectfully submitted that the application is in condition for allowance. Favorable consideration and prompt allowance of claims 1-3 and 5-14 are earnestly solicited. If the Examiner believes that any additional changes would place the application in better condition for allowance, the Examiner is invited to contact the undersigned attorney at the telephone number listed below.

To the extent necessary, a petition for an extension of time under 37 C.F.R. 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this,

concurrent and future replies, including extension of time fees, to Deposit Account 16-0607 and please credit any excess fees to such deposit account.

Respectfully submitted,



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